10-bit Two-Step Single Slope ADC for A Low-Power CMOS Image Sensor

Duhyun Jeon, Don-gu Lee, and Byong-Deok Choi

Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : bdchoi@hanyang.ac.kr

A single slope ADC (SSADC) is widely used for CMOS image sensor because of simple implementation and low area. However, a SSADC requires $2^N$ clocks for N-bit resolution. To overcome this speed limitation, a two-step single slope ADC was proposed with L-bit coarse operation and M-bit fine operation, and $N = L+M$ [1]. Although it reduces the conversion time, it increases power consumption and area because multiple ramp generators are required for fine conversion. These issues can be alleviated by only using a single ramp generator for both coarse and fine operations [2]. In this chip design, a two-step SSADC is designed with single ramp generator. The designed ADC operation is shown in Fig. 1. The timing diagram shows only 2-bit MSB and 2-bit LSB operations for simple description. In coarse conversion, MSB is decided from full-scale $V_{\text{Ramp}}$ and $V_{\text{IN}}$ comparison. When $V_{\text{Ramp}}$ is higher than $V_{\text{IN}}$, control logic samples the voltage difference ($V_{\text{C}}$) between $V_{\text{IN}}$ and $V_{\text{Ramp}}$ to holding capacitor ($C_H$). In fine conversion, this residue is added to reference voltage ($V_{\text{REF}}$) and compared with the fine ramp signal in the range of one MSB. Due to using only residue value in the fine conversion, a single ramp signal can be applied to all column ADC. Because multiple ramp signals are not required for fine conversion, the power consumption can be reduced compared with the case of multiple ramp signals.

Fig 1. Two-step SSADC operation (a) coarse conversion (b) fine conversion (c) timing diagram