Counting-Based Digital-to-Analog Converter Scheme for Compact Column Driver with Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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The concept of a counting-based digital-to-analog converter (CNT-DAC) is proposed to realize a compact column driver circuit for system-on-panel (SoP) applications. The traditional ramp DAC is very promising in the circuit-area respect, because it replaces the area-consuming read only memory (ROM)-type decoder with a counter; however, it is not widely used for display column drivers because it has several problems such as ramp signal distortion, charge sharing between column lines and pixel electrode and ramp signal generation. The CNT-DAC was inspired by the ramp DAC, which uses a counter instead of an area-consuming ROM-type decoder but can avoid the problems mentioned above by using a resistor string at each channel and a global shift register. Instead of designing an 8-bit DAC with the counting-based DAC alone, we combine the 3-bit traditional decoder-based DAC and the 5-bit CNT-DAC, because the 8-bit CNT-DAC needs a clock frequency of about 20 MHz for a portrait qVGA format ($H$: 240, $V$: 320), which is a very difficult requirement to meet. For a 2-in. diagonal portrait qVGA AMOLED panel, the circuit area of one channel DAC is $73 \times 1.010 \times 10^{-6}$ m$^2$ with the design rule of 2 m and a TFT channel length of 4 m. The total power consumption of the CNT-DAC is about 3.2 mW; the static power consumption due to the resistor string at each channel is 1.7 mW, the dynamic power consumption for driving the column lines is about 1.0 mW, and the global shift register consumes about 0.5 mW. [DOI: 10.1143/JJAP.47.1906]

KEYWORDS: DAC, driver circuit, active matrix display, poly-Si TFT

1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology has been intensively researched to integrate row and column driver circuits on glass substrates, and has continued to advance, leading to the concept of a system-on-panel (SoP). The ultimate goal of the SoP device is to fully integrate various types of peripheral circuits including microprocessor, timing controller, memory, DC–DC converter, and interface circuits, as well as row and column driver circuits, on substrates with poly-Si TFTs.1–3) We expect to achieve two benefits from SoP technology. By integrating such peripheral circuits with poly-Si TFTs, we will not need to use integrated circuits (ICs) anymore, so the cost of ICs can be saved. This can contribute to cutting down the total display system cost. In addition, we can also expect to create new concepts for products that have not existed so far, because SoP technology can provide design flexibility, so that the display system developer can design customized circuits without depending on IC suppliers, and can realize a very compact, light-weight, and low-power display system by removing the printed circuit boards (PCBs).

However, SoP technology faces a few challenges. Since the IC cost continues to drop, it appears that the cost benefit of the SoP is very limited. In particular, SoP technology usually requires complementary metal oxide semiconductor (CMOS) process technology (both N- and P-type TFTs), which is not necessarily used when we construct peripheral circuits with ICs. Even worse, the yield of SoP must be lower, because TFT circuits with high complexity are integrated together with pixel arrays. All of these issues can be alleviated by reducing the TFT circuit area, which is surely and directly related to the cost and yield of the SoP device. Of course, compact circuits are essential for minimizing the bezel size around the pixel array for compact, light-weight and low-power display systems.

The issue of circuit area provided the motivation for this research on a compact digital-to-analog converter (DAC).

The column driver circuits of an early stage usually deliver analog video signals, but modern column drivers mostly deal with digital video signals in which digital-to-analog conversion is one of the key functions. Of the various DACs a resistor-string-based DAC (RDAC) is most common, because its operation is very simple, reliable, robust against noises, and compatible with gamma correction. The performance of the DAC scheme has been confirmed over a long time period. However, it has an issue with respect to circuit area. In the case of a 6-bit color depth display, the RDAC scheme uses as many as 6 × 64 TFTs at each channel, constituting about 50% of the area of the column driver circuit. With the increasing requirements concerning the high-quality image displays, the 8-bit or higher color depth has been becoming more common. The 8-bit DAC takes more than four times the area of the 6-bit DAC, because it uses 8 × 256 TFTs at each channel.

The authors previously proposed the concept of a panel DAC that handles a portion of the DAC function with column lines and a hybrid DAC scheme combining the RDAC and the panel DAC.4,5) This panel DAC scheme is very area-efficient and we claim that the scheme works well enough for a 2- or 3-bit DAC without a tough matching requirement on the column line capacitance. Thus, it can provide a very area-efficient 8-bit DAC circuit combined with a 5-bit RDAC. However, the resulting analog signal is subject to some disturbance from the switching error, because the digital-to-analog conversion is basically achieved as a result of switching operation, although the switching error can be suppressed by appropriate circuit design techniques.

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Afterwards, the sampled voltage signal is transferred from the parasitic capacitance of the column line to the pixel electrode at that moment, but is rather delivered to the video data, the sampled voltage is not yet completely considered. Fig. 1(b), when a voltage is sampled by a switch according to the location.

Waveforms arriving at each channel are different depending on the panel and some parasitic resistance and capacitance is inevitable, because the ramp signal line runs across the display area. However, the signal distortion, to some degree, is evident, because the ramp signal integrity cannot be overemphasized for achieving uniformity in the display quality across the entire display area. Therefore, we have to address these three technical issues if we are to apply the traditional ramp DAC scheme to the column driver circuit for a compact circuit area.

3. Operation of Counting-Based DAC (CNT-DAC)

To resolve the aforementioned technical issues of the traditional ramp DAC circuit, we propose a CNT-DAC scheme. The idea and operation principle of the CNT-DAC is explained with an example of a 5-bit DAC in Fig. 2. Each channel of the column driver has a resistor string of 32 resistor segments and two switch arrays, each of which has 32 switches. Every row line time starts with the reset period, during which the shift register simultaneously turns on switches SWB0 to SWB31, and all the capacitors (labeled $C\text{DAC}$) are discharged to ground; then, the switches SWA0 to SWA31 are turned off, because the data input is set to “LOW”. Precharging follows the reset period to charge the column line to the low reference voltage, VRL in Fig. 2, by turning on the switch SWP. Then, the DAC period starts. The shift register sequentially turns on the switches from SWB0 to SWB31. The moment the shift register addresses a right switch corresponding to video data, the data input goes “HIGH”, thus charging the capacitor connected to the switch, which, in turn, turns on the corresponding switch among switches SWA0 to SWA31. The selected voltage on the resistor is output to drive the column line and the pixel circuit. It should be noted that the DAC output voltage is kept constant during the remaining row line time, because the capacitor voltage can keep turning on the switch.

The CNT-DAC is based on a traditional ramp DAC, but we do not have to be concerned about the ramp signal integrity, because it does not depend on the ramp signal running throughout the panel, unlike in the traditional ramp DAC. The increased circuit area for the shift register is very small, since the shift register is shared by all the channels, hence the name global. In addition, the analog voltage is generated using a resistor string, and the adjustment for gamma correction can be easily carried out by selecting appropriate values for resistors. Another advantage is that we can avoid the charge sharing issue, because the DAC output keeps driving the column line and the pixel electrode somewhat deviates from the target voltage.

Lastly, we should add a ramp signal generation circuit to the column driver circuit. This circuit block is not easy to realize with TFTs. Even worse, we need an adjusted ramp signal waveform for gamma correction instead of the linear ramp signal. Thus, it is common to use an external IC for generating the ramp signal as reported in a prior work. Therefore, we have to address these three technical issues if we are to apply the traditional ramp DAC scheme to the column driver circuit for a compact circuit area.

4. Application to Mobile Displays

In this section, we will explain the application of the proposed CNT-DAC to a 2-in. diagonal portrait qVGA ($H$: 240, $V$: 320) AMOLED display. To minimize the peripheral circuit area, the demultiplexing driving scheme is usually used for poly-Si TFT circuits, in which one channel of a column driver drives multiple column lines. However, the
demultiplexing scheme basically shares one channel of a column driver between multiple column lines during a row line time, so the addressing time must be reduced for each column. Thus, the degree of the demultiplexing should be determined with a consideration of the timing margin. A portrait qVGA display with a 60 Hz frame frequency has a row line time of 52 μs. If we apply the 1:2 demultiplexing driving scheme, the addressing time of 26 μs is assigned for each column. As shown in Fig. 2, we need the charging time after the DAC period to charge the pixel electrode to the target voltage. The charging time is strongly dependent on the resistance and capacitance of the row and column signal lines, the TFT performance, and the pixel capacitance. We found from SPICE simulations that a charging time of about 10 μs is necessary for our case. We also have to assign about 4 μs for the reset and precharging periods in Fig. 2. Consequently, about 12 μs can be used for the counting-based DAC operation. If we are to design an 8-bit CNT-DAC, the resistor string composed of 256 resistors has to be scanned for the allocated time of 12 μs, so the global shift register in Fig. 2 has to operate at a frequency of 20 MHz.

Power consumption is one of the most important performance parameters, particularly for mobile displays. Power consumption can be broken down into static and dynamic power consumption. Static power consumption comes from the static currents flowing through the resistor string at each channel, and can be obtained using eq. (1), where $P_{\text{STAT}}$ is the static power consumption, $N_C$ is the number of resistor strings, $V_{\text{DD}}$ is the supply voltage, $I_{\text{RES}}$ is the current flowing through the resistor string, $V_{\text{RES}}$ is the voltage across the resistor string, and $R_{\text{STR}}$ is the resistance of the resistor string.

$$P_{\text{STAT}} = N_C \times V_{\text{DD}} \times I_{\text{RES}}$$

Since we use the 1:2 demultiplexing driving, the number of resistor strings is 360. With the 2 V dynamic range of the

![Fig. 2. (Color online) Circuit and timing diagram of 5-bit counting-based DAC.](image-url)
OLED, the voltage across the resistor string is 0.25 V, because the upper 3-bit chooses two reference voltages for the CNT-DAC from the dynamic range of 2 V as explained in the previous section and Figs. 3 and 5. The resulting static power consumption is roughly 1.7 mW when the resistor string has a resistance of 320 kΩ.

The dynamic power is consumed to charge the capacitance of a column line during each row line time and can be calculated using eq. (2), where \( P_{DYN} \) is the dynamic power consumption, \( I_{AVG} \) is the average current consumed to charge the capacitance of the column line (\( C_L \)), \( V_{SW} \) is the dynamic voltage range of the OLED, and \( F_{ROW} \) is the row-scanning frequency. With a capacitance of 12 pF and a row-scanning frequency of 19.2 kHz, the dynamic power consumption is about 1.0 mW.

\[
P_{DYN} = V_{DD} \times I_{AVG} = N_C \times V_{DD} \times C_L \times V_{SW} \times \frac{F_{ROW}}{2}
\]  

Another power consumption must be considered in the CNT-DAC scheme; the power consumption for the global shift register, which drives switches SWB0 to SWB31 on the signal line running throughout the panel in Fig. 2. To calculate the power consumption, we extracted the parasitic capacitance of the signal line to which the gates of the switches are connected using a RC extraction simulator, RAHPEL. The power consumption is expressed in eq. (3), where \( P_{SHFT} \) is the power consumption of the 32-stage global shift register, and \( C_{SHFT} \) is the capacitance of the signal line. With the extracted capacitance of 12 pF, the
power consumption is estimated to be less than 0.2 mW. However, the global shift register needs a buffer at each output to drive the relatively large capacitive load, signal line and switches, so the power consumption reaches almost 0.5 mW including the power consumed in the buffers. Consequently, the total power consumption of the CNT-DAC consisting of the static and dynamic power consumption, and the global shift register power consumption is about 3.2 mW. The power consumption breakdown and the conditions are given in Table I.

\[ P_{\text{SHIFT}} = C_{\text{SHIFT}} \times V_{\text{DD}}^2 \times F_{\text{ROW}} \]  

5. Simulation and Layout

Figure 6 shows the simulated waveforms of the 8-bit hybrid DAC combining the 3-bit decoder-based DAC and the 5-bit CNT-DAC using HSPICE. After the precharging period, the DAC period follows, during which 32 gray voltages are generated according to the lower 5-bit. Figure 6 shows the 8th, 16th, 24th, and 32nd gray voltages as examples. Although different gray voltages start to rise at different times, all of them have enough time to be delivered to the pixel electrode, because they have the data driving period after the ramp period. It is pretty clear in Fig. 6 that the CNT-DAC scheme is free from the charge sharing issue encountered in the traditional ramp DAC method, and also the switching error, which possibly exists in the authors’ previous hybrid DAC method, because no switching operation is directly involved in generating the analog voltage. The ramp signal distortion issue is also solved, because an analog voltage is generated from a resistor string at each channel.

Figure 7(a) shows a layout diagram of one channel of the 5-bit CNT-DAC circuit. The pixel pitch of a 2-in. portrait qVGA panel is 41 μm, and we use the 1:2 demultiplexing scheme, so the width of the CNT-DAC is determined to be about 82 μm. The holding capacitor in Fig. 7(a) just has to keep the voltage at 1 or 0 for only a row line time, so the capacitance does not need to be so large. Here, the capacitance is optimized to be at 20 pF. The height of the CNT-DAC is just 830 μm. As explained in §4, the CNT-DAC needs an additional control logic composed of five XNOR gates and one 5-input AND gate at each channel. The control logic can be simply constituted by transmission-gate-based logics, and the layout diagram is given in Fig. 7(b), where it is found that the height of the control logic is 180 μm, so the total height of the CNT-DAC is 1,010 μm. Figure 7(c) shows a layout diagram of the global shift register, inverter chains and buffers together with five channels of the CNT-DAC circuits. Because the global shift register should drive a relatively large capacitance of 12 pF, we need relatively large buffers and inverter chains. The total width is about 1,250 μm, and the global shifter registers are used at both ends of the column driver circuits, as shown in Fig. 7(d). We can also move the global shift register to the top of the CNT-DAC with an increase in the circuit height if we do not want the global shift register to be located on the corner area, as shown in Fig. 7(d). The design rule is 2 μm and the channel length of the TFT is 4 μm.

To clearly show the area efficiency of the proposed CNT-DAC, the authors also provide a layout diagram of the conventional ROM-type decoder-based DAC. Figures 8(a) and 8(b) depict a schematic and the layout diagram of the conventional 5-bit ROM-type decoder-based DAC, respectively. Although the CNT-DAC uses a single transistor between a resistor string and a column line, the ROM-type decoder needs five series-connected transistors. Thus, the width of each transistor should be much larger than that of the CNT-DAC to reduce the on-resistance. In our case, the transistor width of the CNT-DAC was 10 μm, but that of the
The ROM-type decoder counterpart was 32 μm. In addition, the conventional one needs ten control signal lines for the 5-bit DAC, which also occupy a relatively large area. The height was approximately 2,220 μm. Thus, the area of the CNT-DAC is 45% of that of the conventional ROM-type decoder-based DAC.

Fig. 7. (Color online) Layout diagram: (a) one-channel counting-based DAC, (b) control logic, (c) global shift register, inverter chains and buffer, and (d) placement of global shift register together with counting-based DAC.

Fig. 8. (Color online) Conventional ROM-type decoder-based DAC: (a) schematic diagram and (b) layout diagram.
6. Conclusions

A concept of a counting-based DAC (CNT-DAC) is proposed for a compact column driver integrated on a panel. This scheme was inspired by the traditional ramp DAC, in that it is based on counting, but solves the issues that the ramp DAC method has: the ramp signal distortion issue due to the parasitic resistance and capacitance of the ramp signal line, the charge sharing between the column line and the pixel electrode, and ramp signal generation. The key idea is to choose an analog voltage from a resistor string at each channel by comparing the video data and the counter output. This is also very advantageous for providing gamma correction. Depending on the TFT performances, the CNT-DAC can be combined with the conventional decoder-based DAC. When the proposed CNT-DAC is applied to a 2-in. diagonal portrait qVGA AMOLED panel with 1:2 multiplexing driving, this work combines the 3-bit decoder-based DAC and the 5-bit CNT-DAC for the qVGA AMOLED, because the operation frequency should be 20 MHz, if we realize an 8-bit DAC with the CNT-DAC method alone. The total power consumption is 3.2 mW, including the static and dynamic values and that of the global shift register. The resulting hybrid 8-bit DAC circuit area is very small, $82 \times 1,140 \mu\text{m}^2$, which is just 45% of that of the conventional ROM-type decoder-based DAC.

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