A True 10-bit Data Driver LSI for HDTV TFT-LCDs

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SUMMARY We present our recent results of the 10-bit data driver LSI for 42-inch diagonal TFT-LCD TV with full HD format. To develop data driver LSIs for a true 10-bit TFT-LCD TV with full HD (1920 × 1080) format, small chip area, low power consumption, and output uniformity between channels are key problems that must be solved. By applying a two-stage DAC which combines 8-bit resistor-string DAC and 2-bit binary weighted capacitor DAC, the area increase is limited to only 30% compared to the area of 8-bit resistor-string DAC. The output deviation between channels is successfully limited within ±5 mV and the driver LSI with 414 outputs consumes the maximum total current of 16 mA when driving 42-inch HDTV panel. We confirmed that the picture with 10-bit shades of gray is much more natural than that with 8-bit shades of gray.

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1. Introduction

TFT-LCD is successfully penetrating into the large-screen TV market. For TV applications, customers want not only the large-size screen and high resolution, but also more natural colors. The color depth of display devices is determined by the number of colors which the device can represent, and the number of colors, in turn, comes from the number of bit of gray scale. Recently, the need of over 10-bit gray scale TFT-LCD is growing in LCD TVs [1]. To develop large-size, high-resolution, and high-gray-scale TFT-LCDs, some design issues must be considered. First, high-speed signaling conventions are needed. As the panel size, resolution, and color depth increase, high-speed data transmission between timing controller and data driver LSIs are required. So, instead of conventional CMOS/TTL signaling, several low-voltage signaling techniques such as mini-LVDS and RSDSTM have been developed [2]–[4]. Second, small chip area should be achieved. The chip area heavily depends on the DAC area because typical 8-bit resistor-string DAC occupies about 60% of the whole driver LSI area, and one bit increase in the data leads to doubling the area of resistor-string DAC. Therefore, to make the chip size small, it is strongly required to reduce the DAC area. Third, output uniformity between channels is another key issue. Because display driver circuits include several hundreds of channels in one chip, channel-to-channel output variations should be minimized to obtain the uniform image quality throughout the entire display area. In [5], technical issues on driver LSI and TFT-LCD panel are discussed for a true 1-billion-color TFT-LCD TV with full HD format.

In this paper, we present the performance of the 10-bit data driver LSI in the view points of DAC area and output uniformity. We also show the evaluation results of the proposed 10-bit gray scale TFT-LCD data driver for 42-inch diagonal HDTV TFT-LCDs.

2. System Architecture of the 10-bit Data Driver LSI for HDTV TFT-LCDs

We designed 10-bit gray scale TFT-LCD data driver LSI. The system block diagram is shown in Fig. 1. The system consists of input stage, control logic, digital-to-analog converter, and output buffer. The mini-LVDS interface is applied for high-speed data transmission. To minimize the area increase of 10-bit resistor-string DAC, a two-stage DAC which combines 8-bit resistor string DAC and 2-bit binary weighted capacitor DAC is chosen. The output buffer can cancel the offset voltages during DA conversion so as to achieve good channel-to-channel uniformity.

Fig. 1 System block diagram of the proposed 10-bit gray scale TFT-LCD data driver LSI.
3. mini-LVDS Interface

We used mini-LVDS interface for high-speed data transfer between T/CON and data driver up to 400 Mbps. Besides high-speed signal conversion, a mini-LVDS input receiver should have a wide input common-mode range specified by (1).

\[ 0.4 V \leq |V_{cm}| \leq 2 V \]  

(1)

![Fig. 2 Circuit diagram of the proposed mini-LVDS receiver.](image)

Fig. 2  Circuit diagram of the proposed mini-LVDS receiver.

where \( V_{cm} \) is the input common-mode voltage of the mini-LVDS receiver. A typical mini-LVDS receiver with only PMOS gate input pair can hardly perform satisfactorily when the supply voltage is less than 3 V and the threshold voltage of MOS devices is 0.5–0.7 V [6]. For this reason, an input receiver with rail-to-rail input common-mode range and high gain-bandwidth product is desirable. Therefore, we newly proposed a mini-LVDS input buffer shown in Fig. 2, with rail-to-rail input common-mode voltage range and dual gain stage which allow wide operating frequency range and high-gain regardless of common-mode voltage and differential voltage variation of input signals. Folded cascode input stage of NMOS input, MN1, MN2, and MN5, covers upper rail of the input common-mode range and folded cascode input stage of PMOS input, MP1, MP2, and MP5, covers lower one. With this dual input stage, the proposed input receiver can cover the rail-to-rail input common-mode range. The next stage of MP8–MP11 and MN8–MN11 is a positive-feedback latch stage. High gain is obtained by the cross-coupled latch composed of MN8 and MN9. Output stage which consists of MP12, MP13 and MN12, MN13 is a typical current mirror type amplifier and this stage converts differential output signal to single-ended signal. Functional test results of the proposed mini-LVDS input buffer are shown in Fig. 3. For input common-mode voltage range between 0.2 V and 2.2 V, the mini-LVDS input buffer recovers CMOS level signals from the low-voltage differential signals.

4. Digital-to-Analog Converter

4.1 Prior Digital-to-Analog Converters

In 8-bit TFT-LCD data driver LSIs using resistor-string type DACs, generally, DAC block occupies over 60% of whole chip area. Most TFT-LCD driver LSIs adopt resistor-string type DACs with decoders as shown in Fig. 4. The resistor-string type DAC is highly efficient for a 64-gray level system in respect of the chip area and yield, but 256-gray level

![Fig. 4 Schematic diagram of typical resistor-string DAC with ROM type decoder.](image)
data driver system with the resistor-string type DAC suffers from impractically large chip area. Here, the gray levels are generated from a resistor-string and fed to the input stage of output buffers through $N$-out-of-$2^N$ switch by ROM type decoder where $N$ is the number of bits of data. In case of these resistor-string type DACs, they need twice as many as switches to increase one bit resolution. For example, if the resistor-string type DAC is applied to 10-bit data driver, then the total DAC area of 10-bit data driver becomes more than 4 times larger than that of 8-bit data driver.

In Fig. 5, examples of various approaches to minimize chip area in 10-bit gray scale DACs. A two-stage resistor-string DAC which combines a 8-bit resistor-string DAC and 2-bit resistor DAC can be one of the solutions for area-efficient 10-bit DAC and it is shown in Fig. 5(a) [7]. But the unity-gain buffers to isolate two resistor-strings might have random offset error caused by process variations so that it is difficult to obtain the output uniformity. To overcome this problem, DAC of Fig. 5(b) has been proposed [8]. The chip area increase of the DAC of Fig. 5(b) is only 29%, but the resistor values of 2-bit resistor-string should be large enough in order not to change the value of 8-bit resistor-string value when 8-bit resistor-string and 2-bit resistor-string are connected in parallel. As in Fig. 5(c), by multiplexing one 10-bit resistor-string DAC with four output channels, the effective DAC area per channel is comparable to that of 8-bit resistor-string DAC [9]. In this case, the only additional circuitries are 4-to-1 multiplexers with extra area of about 20%. But the digital-to-analog conversion time should be fast enough to share one DAC among four output channels. Another 10-bit DAC scheme, shown in Fig. 5(d), is to use 8-bit resistor-string DAC and to integrate 2-bit DAC into an OPAMP. If an OPAMP has four positive input transistors, of which each transistor width is a quarter of that of the negative input transistor as shown in Fig. 5(d), the OPAMP operates as a linear 2-bit DAC. But this idea is valid under the assumption that the random offset of the OPAMP is strictly controlled and the divided positive input transistors are well matched.

4.2 Proposed Digital-to-Analog Converter

In this work, to minimize the area increase of 10-bit resistor-string DAC, a two-stage DAC which combines 8-bit resistor-string DAC and 2-bit binary weighted capacitor DAC is chosen and the circuit diagram is shown in Fig. 6. The 8-bit resistor-string DAC generates two adjacent analog signal outputs and the 2-bit capacitor DAC divides 4 levels between the two adjacent outputs from the 8-bit resistor-string DAC. Each resistor value of 8-bit resistor-string is designed to create gamma-corrected voltage levels and the two adjacent voltage levels are evenly divided to 4 intermediate voltage levels by the binary weighted capacitors in 2-bit capacitor DAC. This DAC has very simple structure and achieves area-efficiency, as the area increase is only 30% compared to the area of 8-bit resistor-string DAC, but it could have some disadvantages such as capacitor mismatch, charge in-

Fig. 5 Various types of DACs. (a) Two-stage resistor-string DAC of 8-bit resistor-string DAC and 2-bit resistor-string DAC with intermediate buffers, (b) two-stage resistor-string DAC of 8-bit resistor-string DAC and 2-bit resistor-string DAC without intermediate buffers, (c) multiplexed type DAC, and (d) 10-bit DAC with a 8-bit resistor-string DAC and 2-bit DAC integrated into an OPAMP.
Fig. 6 Proposed two-stage DAC which combines 8-bit resistor-string DAC and 2-bit binary weighted capacitor DAC (RC-DAC). (a) Conceptual diagram of the proposed two-stage DAC and (b) circuit diagram of the proposed 2-bit binary weighted CDAC.

Injection, and clock feedthrough because it needs capacitors and switches.

The circuit diagram of the proposed 2-bit binary weighted CDAC is shown in Fig. 6(b). It consists of multiplexers to select VRL or VRH according to the input signals, switches to minimize the clock feedthrough and charge injection errors, and output buffer.

The circuit operates in two phases. In the first phase, voltages from resistor-string are decoded. Each node of capacitors, C1 and C2, are connected to VRL regardless of the input signal D0 and D1. Simultaneously, the negative input stage and output stage of OPAMP form a negative feedback. When the offset voltage of the OPAMP is α, the voltages of C0, C1, and C2, are expressed as Eq. (2) to Eq. (4).

\[
V_{C0} = V_{ref} + \alpha - V_{RL} \\
V_{C1} = V_{ref} + \alpha - V_{RL} \\
V_{C2} = V_{RL} - V_{ref} - \alpha
\]

In the second phase, the OPAMP drives TFT-LCD panel, when the nodes of C0 and C1 are connected to VRL or VRH according to D0 and D1 signals. Then, the amount of the voltage difference is delivered to output. Let the selected voltages be \(V_{int0}\) and \(V_{int1}\), respectively, which are the values of VRL or VRH, then the voltages of C0, C1, and C2, have the value of Eq. (5) to Eq. (7).

\[
V_{C0} = V_{ref} + \alpha - V_{int0} \quad (5) \\
V_{C1} = V_{ref} + \alpha - V_{int1} \quad (6) \\
V_{C2} = V_{out} - V_{ref} - \alpha \quad (7)
\]

From Eq. (2) to Eq. (7), \(V_{out}\) can be expressed as Eq. (9).

\[
-C2 \cdot \Delta V_{C2} = C1 \cdot \Delta V_{C1} + C0 \cdot \Delta V_{C0} \quad (8)
\]

\[
V_{out} = V_{RL} \left(1 - \frac{C0 + C1}{C2}\right) + \frac{C1}{C2} V_{RH} + \frac{C0}{C2} V_{RL} \quad (9)
\]

Note that in Eq. (9) that the offset voltage, \(\alpha\), is cancelled.

5. Output Buffer

Generally, unity-gain buffer is used as an output buffer of TFT-LCD driver circuits. It is desired that the output buffer should have the characteristics of rail-to-rail operation range in input and output, low-power consumption, high slew rate, and especially, high output uniformity between channels.

In display driver LSIs, generally, each column has its own buffer, so several hundreds of output buffers are included in a driver LSI. Consequently, the output buffers take a big part of power consumption of a driver LSI. Assuming that the quiescent current of an output buffer is as low as 10 \(\mu\)A, the number of channels is 414, the power consumption with a 18 V supply is then \(10 \mu A \times 414 \times 18 V = 74.52 mW\), and it should be noted that this power consumption only accounts for the static current of the output buffers not including the panel AC driving power consumption. Moreover, because the slew rate of an output buffer is proportional to the bias current, trade-off between bias current and slew rate should be made. Unfortunately, the fact that low quiescent current and high slew rate output buffer is necessary for TFT-LCD driver circuits pose a great challenge on designing output buffers.

To satisfy those requirements above, low-power consumption and high-slew-rate OPAMP has been designed. When input pulse, which swings 0.2 V to 14.8 V, with the supply voltage of 15 V, the measured slew rate is 3.7 V/\(\mu\)sec at the quiescent current of 8 \(\mu\)A when the load resistance is 21.9 k\(\Omega\) and the load capacitance is 151 pF. It also provides push-pull operation required for dot inversion to express high-quality images.

Not only the low quiescent current and high slew rate, but the output uniformity between channels is important for TFT-LCD driver circuits. To maintain the channel-to-channel or chip-to-chip output error less than a few mili-volts, the output buffer must have an offset cancellation function. In this work, we achieve the offset cancellation as described in Sect. 4.1.
6. Evaluation of the 10-bit Data Driver

We successfully developed a true 10-bit gray scale TFT-LCD data driver LSI for 42-inch diagonal and HD format TFT-LCD TV application using a 3.3 V/18 V 0.35 μm 2poly/4 metal CMOS technology. Its number of output is 384-/414-channel selectable. The driver LSI with 414 outputs consumes the total current of 16 mA when driving 42-inch HDTV panel. The chip area is 16,000 × 3,300 μm², and that is just 30% increase of that of the conventional 8-bit data driver with the same output channels. And its output offset voltage level is less than ±5 mV. Figure 7 shows experimental results of demonstration images. We confirmed that the picture with 10-bit shades of gray is much more natural than that with 8-bit shades of gray.

7. Conclusions

A True 10-bit TFT-LCD data driver LSI using a two-stage DAC which combines 8-bit resistor-string DAC and 2-bit binary weighted capacitor DAC with mini-LVDS interface for 42-inch diagonal and full HD format TFT-LCD TV applications is proposed. The area increase of the proposed 10-bit data driver LSI is only 30% of that of the conventional 8-bit resistor-string DAC. The output deviation is successfully limited within ±5 mV. The proposed 10-bit TFT-LCD data driver can represent much more precise and natural colors than conventional 8-bit data driver can.

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References


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